MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2019/2020

EEN 1036 - DIGITAL LOGIC DESIGN

(TE/RE)

5 MARCH 2020
9.00 a.m. - 11.00 a.m.
(2 Hours)

INSTRUCTION TO STUDENT

1. This question paper consists of 5 pages (including cover page) with 4 questions.
2. Attempt **ALL** questions. All questions carry equal marks and the distribution of the marks for each question is given.
3. Please write all your answers in the answer booklet provided.

QUESTION 1

(a) In science, technology and in fact most field of endeavor, we are constantly dealing with *quantities*. It is important that we are able to represent various quantities efficiently and accurately. There are basically two ways of representing the numerical value of quantities: analog and digital.

i. Discuss the difference between a digital quantity and an analog quantity.

[2 marks]

ii. List two products that measure analog quantities.

[2 marks]

iii. Digital representation has certain advantages over analog representation in electronics applications. State four advantages of digital techniques over analog.

[4 marks]

(b) Perform the following operations in 2's complement system by using 8 bits (including the sign bit) for each number. Verify your answers in decimal number system.

i. Add -46_{10} from 23_{10}
ii. Subtract 98_{16} from $A5_{16}$

[4 + 4 marks]

(c) Convert the following. Show your working.

i. 153_8 to Gray code
ii. 001111 Gray code to Binary

[3 + 2 marks]

(d) A transmitter will send the number 51_{10} to a receiver.

i. Assuming that it is an odd parity system, convert 51_{10} into 8-bit binary numbers and assign proper odd parity bit to the number.

[2 marks]

ii. Assuming that the data received is contaminated by noise and the least significant bit of the number is in error. Explain how the receiver detect the error.

[2 marks]

Continued...

QUESTION 2

Given a logic circuit as shown in Figure Q2,

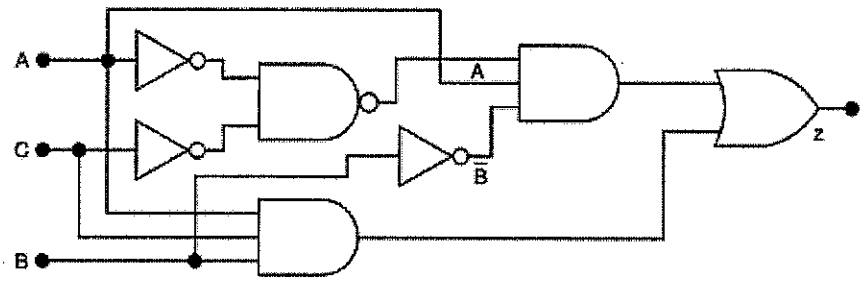


Figure Q2

(a) Determine the Boolean expression for the circuit.

[2 marks]

(b) Simplify the expression using DeMorgan's theorem.

[4 marks]

(c) Draw the logic circuit diagram for the simplified expression.

[4 marks]

(d) Construct the truth table for the Boolean expression for the circuit.

[4 marks]

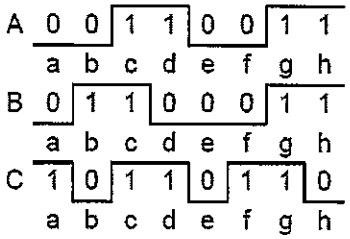
(e) Write out the maxterm Boolean expression for z from the truth table.

[2 marks]

(f) From the maxterm Boolean expression obtained, demonstrate how a Karnaugh map (K-map) can be used to obtain the simplified expression in (b). Show your working.

[7 marks]

(g) If the inputs A, B and C are varying according to the timing diagram below, what should be the waveform at z?



[2 marks]

Continued...

QUESTION 3

Design a **MOD 5 SYNCHRONOUS UP COUNTER** using J-K flip-flops by answering the following questions:

(a) Draw its state diagram.

[1 mark]

(b) Draw its state-transition table.

[10 marks]

(c) Minimize the logic using K-map.

[10 marks]

(d) Implement the design by drawing its logic diagram.

[4 marks]

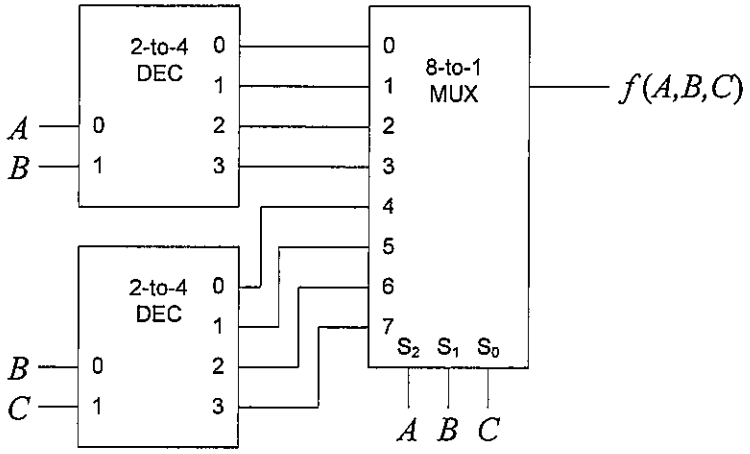
Continued...

QUESTION 4

(a) Implement the functions $f_1(X_2, X_1, X_0) = \prod M(1, 2, 3, 6, 7)$ and $f_2(X_2, X_1, X_0) = \prod M(0, 1, 3, 4, 5)$ using OR-gates along with a 3-to-8 decoder. (Note that X_2 is the most significant bit whereas X_0 is the least significant bit.)

[7 marks]

(b) Consider the following circuit:



Note that A is the most significant bit whereas C is the least significant bit.

i. Draw the truth table and hence suggest a practical use for the circuit above.

[4 + 2 marks]

ii. With appropriate standard gates and a 2-to-1 multiplexer, design an equivalent circuit.

[4 marks]

(c) A full adder (FA) is a multiple-output combinational logic network that adds three binary bits, i.e., two data bits (A and B) and one carry-in bit (C_0), produces a sum bit (S) and a carry-out bit (C_1) output signals.

i. Draw the truth table for a FA. [4 marks]

ii. Implement a FA using a 1-to-8 demultiplexer with active-high outputs and appropriate standard gates.

[4 marks]

End of Paper